REMARKS

This Amendment is submitted in response to the Examiner's Action mailed January 14, 2005, with a shortened statutory period of three months set to expire April 14, 2005. Claims 1-23 are currently pending.

Applicants' claims describe routing data packets to multiple partitions within a single end node. A range of local identification addresses (LIDs) are assigned to a channel adapter port in an end node. Bits within the local identification addresses are assigned to specify which of several partitions within the end node is being addressed.

The Examiner rejected claims 1-23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,694,361 issued to *Shah* in view of Official Notice. This rejection is respectfully traversed.

Regarding the independent claims, Applicants claim routing data packets to multiple partitions within a single end node. The Examiner states that *Shah* teaches routing packets to multiple partitions by teaching a partition manager at column 7, lines 37-41. *Shah* does teach a partition manager that assigns partition keys to fabric agents at column 7, lines 37-41. However, *Shah* provides no other teaching regarding partitions other than the statement that "Examples may include a partition manager that assigns partition keys to fabric agents." Column 7, lines 37-41. *Shah* does not teach routing packets to multiple partitions. The statement in *Shah* that a partition manager assigns partition keys to fabric agents does not teach routing packets to multiple partitions. Therefore, *Shah* does not teach this feature of Applicants' claims.

Applicants claim assigning a range of local identification addresses (LIDs) to a channel adapter port in an end node. The Examiner states that *Shah* teaches assigning a range of LIDs to a channel adapter port in Figure 6 and column 8, lines 42-51. *Shah* teaches assigning a LID to a port where the LID is used as an address to route messages from a source port to the destination port in the fabric. *Shah* also teaches that a port can be assigned multiple LIDs where each LID for a port specifies a different path to that port from some other port on the fabric. *Shah* does not teach, however, assigning a range of LIDs to a port. Applicants claim assigning a range of LIDs to a port. Assigning multiple

LIDs is not the same thing as assigning a range of LIDs. Therefore, *Shah* does not teach assigning a range of LIDs to a port.

Applicants claim assigning bits within the local identification addresses to specify which of several partitions within the end node is being addressed. The Examiner states that *Shah* teaches assigning a value within the LID to specify which of several partitions is being addressed. The Examiner refers to column 10, lines 49-54 as teaching assigning a value within a LID. This section of *Shah* teaches the subnet manager maintaining a tunable parameter called a "LID stride value". This parameter indicates the minimum separation between the LIDs assigned to different ports. "For example, if the LID stride value is 16, then each detected port is assigned a LID value such that the absolute difference between the LID values of any two ports is a multiple of 16. If four ports are detected on the fabric, the initial base LIDs assigned could be 1, 17, 33, and 40. LIDs that fall in between LID stride values are not initially assigned." Column 10, lines 49-55.

Applicants claim assigning bits within the LID itself. The LID stride value taught by *Shah* is the amount of difference between one LID and another LID. The LID stride value does not teach assigning bits in any way. The LID value does not teach assigning bits within the LID itself. The LID stride value is merely a difference between one LID and another. The difference between one LID and another is not the same thing as assigning bits within the LID itself. Therefore, *Shah* does not teach this feature of Applicants' claims.

The LID stride value of *Shah* also does not teach assigning a value to a LID. The LID stride value of *Shah* is not a LID value. The LID stride value is a permitted difference between LIDs. It is not a value that is assigned to a LID.

Regarding specifying which partition is being addressed, the Examiner refers to column 8, lines 42-51 as teaching each port being uniquely identified. Applicants claim assigning bits within the local identification addresses to specify which of several partitions within the end node is being addressed. The Examiner refers to a section of *Shah* that teaches each port being uniquely identified. This section of *Shah* does not teach bits within a LID being used to specify which partition is being addressed. *Shah* teaches using the LID to specify a port, not a partition. *Shah* does not teach using bits

within a LID to specify which one of several partitions is being addressed. Therefore, *Shah* does not teach this feature of Applicants' claims.

The Examiner states that *Shah* does not teach assigning bits within a LID but takes Official Notice that the concept of bit masking is well known. The Examiner further states that one of ordinary skill in the art would recognize that assigning logical significance to particular bits would optimize processing. However, assigning logical significance to particular bits would not teach this feature of Applicants' claims. Assigning logical significance to particular bits would not teach assigning bits within the local identification addresses to specify which of several partitions within the end node is being addressed. Assigning logical significance to a bit is not the same as specifying which of several partitions is being addressed.

The Examiner relies on *Shah* to teach particular individual features of Applicants' claims. However, *Shah* does not teach the individual features of Applicants' claims and also does not teach the particular combination of features claimed by Applicants. *Shah* does not teach (1) routing data packets to multiple partitions, (2) a range of local identification addresses (LIDs) being assigned to a channel adapter port in an end node, or (3) bits within the local identification addresses being assigned to specify which of several partitions within the end node is being addressed. The combination of *Shah* and the Official Notice does not render Applicants' claims unpatentable because the combination of *Shah* and the Official Notice does not describe, teach, or suggest (1) routing data packets to multiple partitions, (2) a range of local identification addresses (LIDs) being assigned to a channel adapter port in an end node, or (3) bits within the local identification addresses being assigned to specify which of several partitions within the end node is being addressed.

Regarding claims 2 and 10, Applicants claim the bits that are assigned within the LID to specify which of several partitions is being addressed being lower order bits. The Examiner states that *Shah* teaches this feature at column 10, lines 49-54. However, the Examiner also stated in paragraph 4 of the Office Action that *Shah* did not teach assigning bits within the LIDs. Therefore, *Shah* cannot teach assigning lower order bits when the Examiner admits that *Shah* does not assigning bits at all.

Further, the referenced section of *Shah* does not teach assigning bits. The referenced section teaches a LID stride value. As discussed above, the LID stride value does not teach assigning bits in the LID itself. Therefore, *Shah* does not render Applicants' claims unpatentable.

Regarding claims 5, 13, and 20, Applicants claim the lower order bits assigned to partitions being designated by a local identification mask control (LMC) field. The Examiner states that *Shah* teaches this feature at column 10, lines 49-54, specifically referring to the multiple of 16 described in *Shah*. However, the Examiner also stated in paragraph 4 of the Office Action that *Shah* did not teach assigning bits within the LIDs. Therefore, *Shah* cannot teach assigning lower order bits where the bits are designated by an LMC field when the Examiner admits that *Shah* does not assigning bits at all.

Further, the referenced section of *Shah* does not teach lower order bits assigned to partitions being designated by a local identification mask control (LMC) field. The referenced section teaches a LID stride value that may be 16. This value of 16 is the required difference between LIDs. The value of 16 is not used as a mask field. As discussed above, the LID stride value does not teach assigning bits in the LID itself. Further, the LID stride value does not teach lower order bits assigned to partitions being designated by a local identification mask control (LMC) field. Therefore, *Shah* does not render Applicants' claims unpatentable.

Regarding claims 6, 14, and 21, Applicants claim the LID mask control being any number of bits. The Examiner states that *Shah* teaches this feature at column 10, lines 49-54, specifically referring to the multiple of 16 described in *Shah*. However, the Examiner also stated in paragraph 4 of the Office Action that *Shah* did not teach assigning bits within the LIDs. Therefore, *Shah* cannot teach assigning lower order bits where the bits are designated by an LMC field and the LID mask control being any number of bits when the Examiner admits that *Shah* does not assigning bits at all.

Further, the referenced section of *Shah* does not teach the LID mask control being any number of bits. The referenced section teaches a LID stride value that may be 16 although the value could be different. However, a different LID stride value still would not teach a mask field or the LID mask control being any number of bits. Therefore, *Shah* does not render Applicants' claims unpatentable.

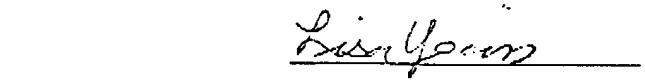
Regarding claims 7, 15, and 22, Applicants claim a number of lower order bits assigned to addressing within a port is up to two raised to the local identification mask control power. The Examiner states that *Shah* teaches this feature at column 10, lines 49-54, specifically referring to the multiple of 16 described in *Shah*. However, the Examiner also stated in paragraph 4 of the Office Action that *Shah* did not teach assigning bits within the LIDs. Therefore, *Shah* cannot teach a number of lower order bits assigned to addressing within a port is up to two raised to the local identification mask control power when the Examiner admits that *Shah* does not assigning bits at all. Therefore, *Shah* does not render Applicants' claims unpatentable.

Regarding claims 8, 16, and 23, Applicants claim the different local identification addresses of a port identifying different partitions within the end node. The Examiner states that *Shah* teaches this feature at column 8, lines 42-51. As described above, *Shah* does not teach the different LIDs of a port identifying different partitions.

The combination of *Shah* and the Official Notice does not render Applicants' claims unpatentable because the combination does not describe, teach, or suggest (1) routing data packets to multiple partitions, (2) a range of local identification addresses (LIDs) being assigned to a channel adapter port in an end node, or (3) bits within the local identification addresses being assigned to specify which of several partitions within the end node is being addressed. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 04.14.05

Respectfully submitted,



Lisa L.B. Yociss
Reg. No. 36,975
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants